Amendments to the Claims

1. (*Currently Amended*) A dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising a cascade of dual residue converter stages ~~(S1 ... SN)~~, the first of said stages ~~(S1)~~ comprising

means to receive the analog input signal ~~(I)~~, means ~~(G1)~~ to derive one or more digital bits ~~(D1)~~ from said analog input signal and

means ~~(H1)~~ to generate first and second residue signals ~~(A1, B1)~~ representing the quantization error left after the AD-conversion of said first stage, each of the following stages ~~(S2 ... SN)~~ in the cascade of dual residue converter stages comprising means to receive the first and second residue signals ~~(A1 ... AN-1, B1 ... BN-1)~~ generated by the previous stage in the cascade, means ~~(G2 ... GN)~~ to derive one or more further digital bits ~~(D2 ... DN)~~ from said received first and second residue signals and each of said following stages except the last one in the cascade comprising means ~~(H1 ... HN-1)~~ to generate first and second residue signals ~~(A2 ... AN-1, B2 ... BN-1)~~ representing the quantization error left after the AD-conversion of the stage, characterized in that each of the stages ~~(S1 ... SN-1)~~ of the dual residue pipelined AD-converter, except the last one, comprises switched capacitor means for the generation of the first and second residue signals ~~(A1 ... AN-1, B1 ... BN-1)~~.

2. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in claim 1 characterized in that each of said following stages except the last one comprise input capacitors ~~(C3 ... C6)~~ for receiving during a sampling phase the first and second residue signals generated by the previous stage, switching means (φ) to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors ~~(C'3, C'4)~~, and means to generate first and second residue signals ~~(A2, B2)~~ from said first and second output capacitors ~~(C'3, C'4)~~ respectively.

3. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in claim 2 characterized in that said switching means (φ) are arranged to transfer charge from said first received residue signal ~~(A1)~~ to said first output capacitor ~~(C'3)~~ with a gain factor of approximately 2 and charge from both said first ~~(A1)~~ and second ~~(B1)~~ received residue signals to said second output capacitor ~~(C'4)~~ each with a gain factor of approximately 1 in a first sub-range mode ($D_2 = 0$) and to transfer charge from said second received residue signal ~~(B1)~~ to said second output capacitor ~~(C'4)~~ with a gain factor of approximately 2 and charge

from both said first ~~(A1)~~ and second ~~(B1)~~ received residue signals to said first output capacitor ~~(C'3)~~ each with a gain factor of approximately 1 in a second sub-range mode (D_2 = 1).

4. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in claim 3 characterized in that said switching means are additionally arranged to transfer charge from both said first ~~(A1+, A1-)~~ and second ~~(B1+, B1-)~~ received residue signals to said first output capacitor ~~(2C'17)~~ with a gain factor of approximately 3/2 and 1/2 respectively and charge from both said first ~~(A1+, A1-)~~ and second ~~(B1+, B1-)~~ received residue signals to said second output capacitor ~~(2C'18)~~ with a gain factor of approximately 1/2 and 3/2 respectively in a third sub- range mode (E = 1) which lies symmetrically between said first and second sub-range modes.

5. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in claim 2 characterized in that for the generation of each residue signal ~~(A2, B2)~~ an operational amplifier ~~(J3, J4)~~ is provided and that each output capacitor ~~(C'3, C'4)~~ is connected during the tracking phase (φ) between an output terminal and the inverting input terminal of said operational amplifier.

6. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in claim 5 characterized in that one side of each input capacitor ~~(2C19 ... C30)~~ is connected to said inverting input terminal both during the sampling phase (φ) and during the tracking phase (φ) and that each output capacitor ~~(C'13 ... C'16)~~ is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier ~~(J9, J10)~~.

7. (*Currently Amended*) A dual residue pipelined AD-converter as claimed in ~~any of the preceding claims~~claim 1, characterized in that in that the switched capacitor means are arranged to receive balanced first and second residue signals ~~(A1+, A1-, B1+, B1-)~~ and to generate there from balanced first and second residue signals ~~(A2+, A2-, B2+, B2-)~~ for application to the next stage in the cascade.